JESD204B & JESD204C

A Comprehensive Annotated Bibliography

Standards, Application Notes, Whitepapers and Peer-Reviewed Research

2010 – 2026

The JEDEC JESD204 family of serial data-converter interfaces has reshaped how high-speed ADCs and DACs connect to FPGAs and ASICs in radar, 5G/6G infrastructure, software-defined radio, instrumentation, medical imaging and quantum-control systems. This bibliography compiles the primary normative documents from JEDEC, including the most recent JESD204D (December 2023) revision, the principal application notes and white papers from Analog Devices, Texas Instruments, AMD/Xilinx and Intel/Altera, and a selection of peer-reviewed academic work characterising and extending the standard.

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Contents

1 Introduction and Scope

The JESD204 standard, first published by the Joint Electron Device Engineering Council (JEDEC) in April 2006, defines a serialised, point-to-point interface between high-speed data converters (ADCs and DACs) and logic devices such as FPGAs, ASICs and DSPs. Successive revisions, JESD204A (April 2008), JESD204B (July 2011), JESD204C (December 2017, with errata JESD204C.01 in December 2021), and most recently JESD204D (December 2023), have raised the per-lane line rate from 3.125 Gbps to 116 Gbps (PAM4) / 58 Gbps (NRZ), introduced deterministic latency, added the more efficient 64B/66B and 64B/80B link layers alongside the legacy 8B/10B layer, and, in the D revision, introduced Reed-Solomon FEC, three channel-reach categories (XSR/MR/LR) and a revised subclass set in which Subclass 2 is removed and the former Subclass 1 MULTIREF operation is renamed Subclass 3.

This bibliography is structured into three parts:

- **Part A, Normative Standards** (JEDEC documents and immediate primer literature).
- **Part B, Application Notes and White Papers** (Analog Devices, Texas Instruments, AMD/Xilinx, Intel/Altera).
- **Part C, Peer-Reviewed Research and Academic Papers** (IEEE Xplore, MDPI, arXiv, conference proceedings).

A consolidated comparison table summarising the key technical differences between JESD204B and JESD204C closes the document. (The companion LaTeX source file preserves a more extensive three-way table including JESD204D as a commented-out alternative for future activation.)

Revision 1.1 (July 2026). Technical corrections after re-verification against JESD204C.01 and JESD204D: JESD204C maximum lane rate corrected to 32.45 Gbps; JESD204D backward-compatibility and subclass statements aligned with Annex A.1 of the standard (RS-FEC link layer not backward compatible, Subclass 2 removed, Subclass 3 renamed from ”Subclass 1 using MULTIREF”); N’ padding corrected from octet to nibble granularity; the 500 MSPS subclass boundary reattributed to vendor literature versus the informative Annex B device-clock recommendation; two ADI subclass articles added; citation defects repaired (LiteJESD204B authorship, one broken DOI placeholder). All URLs were last verified on July 2, 2026.

Note on access. The JEDEC standards themselves are normative documents distributed by JEDEC under registration; abstracts are public, full text is licensed. All other entries link to publicly available URLs or DOIs. Where a DOI was not assigned (most vendor literature), the canonical URL is given.

2 Part A: Normative Standards (JEDEC)

[1] **JESD204D (December 2023)**
Title: Serial Interface for Data Converters
Standard ID: JESD204D
Publisher: JEDEC Solid State Technology Association, Arlington, VA, USA
Publication Date: December 2023
Type: Normative standard (current revision)
URL: https://www.jedec.org/standards-documents (JESD204D; full text after free registration, no stable per-document deep link)
Abstract. The current revision of the JESD204 family. Per the official JEDEC abstract, JESD204D *"describes a serialized interface between data converters and logic devices. It contains normative information to enable designers to implement devices that communicate with other devices covered by this specification. Informative annexes are included to clarify and exemplify the document."* The principal technical advances over JESD204C are: 1. The introduction of PAM4 signalling alongside the legacy NRZ (PAM2) physical layer, raising the per-lane data rate to up to 116 Gbps PAM4 / 58 Gbps NRZ. 2. Reed-Solomon Forward Error Correction (RS-FEC) replacing the JESD204C Fire code, mandatory for PAM4 links because of the elevated raw bit-error rate, and used in NRZ mode for error *detection* in place of CRC. 3. A new framing scheme oriented around FEC code words, with Sync Header Bursts replacing the per-block sync-header bits used for boundary detection in JESD204C. 4. Three defined channel-reach classes, Extra-Short-Reach (XSR), Medium-Reach (MR) and Long-Reach (LR). 5. A new *Subclass 3* formalising the MULTIREF mechanism (which existed informally in JESD204C but had no subclass designation), allowing multi-device alignment on a common Local Alignment Clock (LAC) when SYSREF is unavailable, although Subclass 3 does *not* provide deterministic latency. 6. New link-layer parameters (notably P, the number of payload octets per FEC code word). The transport layer is unchanged from JESD204B/C, preserving multi-converter alignment over multi-lane links, and is backward compatible with previous revisions. The RS-FEC link layer itself, however, is not backward compatible with any prior JESD204 link layer (Annex A.1); interoperability with JESD204C.01 and JESD204B is achieved at the device level by retaining the earlier link layers as separate operating modes. Revision D also removes all references to Subclass 2 and renames the former "Subclass 1 using MULTIREF" operation to Subclass 3. The full text is licensed material distributed by JEDEC.

[2] **JESD204C.01 (December 2021)**
Title: Serial Interface for Data Converters (Revision/Errata of JESD204C)
Standard ID: JESD204C.01
Publisher: JEDEC, Arlington, VA, USA
Publication Date: December 2021
Type: Normative dot-revision (errata to JESD204C)
URL: https://www.jedec.org/standards-documents (JESD204C.01; full text after free registration, no stable per-document deep link)
Abstract. A dot-revision of JESD204C published four years after the original C revision. JEDEC dot-revisions carry editorial corrections and clarifications without changing the normative scope; JESD204C.01 should be treated as the canonical reference for any new design that targets the C revision (and remains the backward-compatibility target for 64B/66B operation at up to 32.45 Gbps).

[3] **JESD204C (December 2017)**
Title: Serial Interface for Data Converters
Standard ID: JESD204C
Publisher: JEDEC, Arlington, VA, USA
Publication Date: December 2017
Type: Normative standard (superseded by JESD204C.01 / JESD204D for new designs)
URL: https://www.jedec.org/standards-documents/docs/jesd204c
Abstract. Third-generation revision of the JESD204 serial interface, raising the per-lane line rate to 32.45 Gbps (supported raw bit rates range from 0.3125 Gbps to 32.45 Gbps). Adds two new link layers (64B/66B, based on IEEE 802.3 clause 49, and 64B/80B retaining 8B/10B clocking ratios) alongside the legacy 8B/10B link layer for backward compatibility. Introduces mandatory scrambling for the 64-bit link layers, optional Forward Error Correction via a Fire code that corrects up to 9-bit burst errors per multiblock, the Extended Multiblock structure for synchronisation, the JESD204 Channel Operating Margin (JCOM) compliance metric, and reorganises the document into Introduction/Common Requirements, Physical Layer, Transport Layer, and per-link-layer sections.

[4] **JESD204B (July 2011)**
Title: Serial Interface for Data Converters
Standard ID: JESD204B
Publisher: JEDEC, Arlington, VA, USA
Publication Date: July 2011
Type: Normative standard
URL: https://www.jedec.org/sites/default/files/docs/JESD204B.pdf (official JEDEC-hosted PDF); archived copies of this URL: https://web.archive.org/web/*/https://www.jedec.org/sites/default/files/docs/JESD204B.pdf
Abstract. Defines the second-generation high-speed serial interface between data converters and logic devices. Specifies multi-lane support up to 12.5 Gbps per lane using 8B/10B encoding, three subclasses (Subclass 0: backward-compatible, no deterministic latency; Subclass 1: SYSREF-based deterministic latency; Subclass 2: SYNC~-based deterministic latency), the Initial Lane Alignment Sequence (ILAS), the local multiframe clock (LMFC), and the use of CML drivers in place of LVDS. The informative Annex B recommends the Subclass 1 (SYSREF) approach for device-clock rates above approximately 500 MHz; the widely quoted "500 MSPS" subclass boundary is a vendor simplification of this device-clock recommendation, not a normative limit. The most widely deployed revision in fielded designs.

[5] **JESD204A (April 2008)**
Title: Serial Interface for Data Converters, Revision A
Standard ID: JESD204A
Publisher: JEDEC, Arlington, VA, USA
Publication Date: April 2008
Type: Normative standard (historical, included for completeness)
URL: https://www.jedec.org/standards-documents/docs/jesd-204a
Abstract. First revision of the original JESD204 (April 2006). Extends the single-lane single-converter scope of the original specification to support multiple lanes per link and multiple converters per device. Lane synchronisation features were added but no deterministic-latency mechanism was defined. Largely superseded by JESD204B Subclass 0, but cited as the foundation document on which all subsequent revisions build.

Background Reference: JESD204D

Because JESD204D was published only in December 2023, the supporting industry literature is still emerging. The two most substantive public-domain references at the time of compilation are listed here as a supplement to the normative standards above.

[6] **Comcores: Predictions and Expectations of the Upcoming JESD204D Standard**
Author: P. Ovenden (member of JEDEC TG16-4 Task Group), Comcores ApS
Type: Industry analysis from a TG16-4 task-group member
Date: 2023 (pre-publication preview); updated post-publication
URL: https://www.comcores.com/predictions-for-jesd204d/
Abstract. Authored by a member of the JEDEC TG16-4 task group responsible for JESD204D, this article previews and then reviews the principal new features: PAM4 signalling at up to 58 Gbaud (116 Gbps), retained NRZ at up to 58 Gbps, mandatory RS-FEC for PAM4, FEC-code-word-oriented framing with Sync Header Bursts, the new Subclass 3 (MULTIREF / Local Alignment Clock), and the new link-layer parameter P (payload octets per FEC code word). Notes that the transport layer is unchanged and MCDA-ML alignment is preserved.

[7] **Logic Fruit Technologies: From JESD204B to JESD204D**
Title: From JESD204B to JESD204D, The Evolution of High-Speed Data Interfaces
Publisher: Logic Fruit Technologies (Technical Blog)
Date: 2024
Type: IP-vendor educational article
URL: https://www.logic-fruit.com/blog/high-speed-interface/from-jesd204b-to-jesd204d/
Abstract. A vendor-neutral overview of the four published revisions (B/C/C.01/D), summarising lane rates, encoding schemes, FEC strategies and the role of RS-FEC in compensating for the elevated PAM4 raw BER. Useful as a teaching resource for engineers migrating designs from B to D. —

3 Part B: Application Notes and White Papers

3.1 Analog Devices

[8] **J. Harris: JESD204B Survival Guide**
Author: Jonathan Harris
Publisher: Analog Devices, Inc., Norwood, MA, USA
Date: 2013
Type: Compendium of technical articles (~50 pages)
URL: https://www.analog.com/media/en/technical-documentation/technical-articles/JESD204B-Survival-Guide.pdf
Abstract. A practitioner-oriented compendium that collates the main MS-series technical articles from Analog Devices into a single PDF. Covers the protocol overview, JESD204B versus serial LVDS, the physical-layer (PHY) performance metrics, multi-ADC synchronisation, the ABCs of interleaved ADCs, troubleshooting techniques using oscilloscopes and logic analysers, and link-bring-up procedures with Xilinx ChipScope and Altera SignalTap. The most widely cited single resource for engineers approaching JESD204B for the first time.

[9] **I. Beavers: Demystifying Deterministic Latency Within JESD204B Converters**
Author: Ian Beavers
Publisher: Analog Devices Technical Article MS-2626 / *Electronic Design*
Date: February 2014
URL: https://www.analog.com/en/resources/technical-articles/demystifying-deterministic-latency-within-jesd204b-converters.html
Abstract. Explains how deterministic latency is established across an array of JESD204B converters, with emphasis on the role of SYSREF in latching the local multiframe clock (LMFC) at transmitter and receiver, the alignment of samples to frame boundaries, and the deskew procedure required when interleaved or phase-coherent multi-ADC sampling is required. Provides a Q&A-style walk-through of the most common system-design questions.

[10] **ADI: JESD204B Subclasses, Part 1: An Introduction to JESD204B Subclasses and Deterministic Latency**
Author: Analog Devices, Inc. (Technical Article)
Publisher: Analog Devices, Inc. / *Electronic Design*
URL: https://www.analog.com/en/resources/technical-articles/jesd204b-subclasses-part1-an-introduction-to-jesd204b-subclasses-and-deterministic-latency.html
Abstract. Defines deterministic latency as the sum of fixed and variable delays, the latter arising from arbitrary clock-domain phase relationships between power cycles, and introduces the three JESD204B subclasses against this background. Documents the pre-JESD204B practice of implementing deterministic latency in external application-layer circuitry and describes an application-layer synchronisation workaround for Subclass 0 systems. Companion to Part 2 below.

[11] **ADI: JESD204B Subclasses, Part 2: Subclass 1 vs. Subclass 2 System Considerations (MS-2677)**
Author: Analog Devices, Inc. (Technical Article MS-2677)
Publisher: Analog Devices, Inc. / *Electronic Design*
URL: https://www.analog.com/en/resources/technical-articles/jesd204b-subclasses-part-2-subclass-1-vs-subclass-2-system-considerations.html
Abstract. Introduces deterministic latency uncertainty (DLU) as the LMFC skew of a JESD204B system, bounded by the earliest and latest possible SYSREF capture. Analyses SYSREF setup and hold timing, the advantage of source-synchronous clocking in Subclass 1 over the system-synchronous clocking of Subclass 2, and the device-clock frequency limits that restrict Subclass 2 to lower-rate systems. Directly complements the informative Annex B device-clock guidance in [4] and quantifies the sample-accurate DLU target of plus/minus one half sample clock.

[12] **H. Sun: Quickly Implement JESD204B on a Xilinx FPGA**
Author: Haijiao Sun
Publisher: *Analog Dialogue*, vol. 49, Analog Devices, Inc.
Date: September 2015
URL: https://www.analog.com/en/resources/analog-dialogue/articles/quickly-implement-jesd204b.html
Abstract. Describes the four protocol layers (transport, optional scrambling, data-link, physical) and how they map onto the Xilinx LogiCORE JESD204 IP and the GTP/GTX/GTH gigabit transceivers in 7-Series and UltraScale devices. Provides a simplified design example that strips away the AXI configuration overhead present in the vendor reference design and offers practical guidance on clocking, SYSREF capture and reset sequencing.

[13] **D. Jones: JESD204C Primer: What's New and in It for You, Part 1**
Author: Del Jones
Publisher: *Analog Dialogue*, Analog Devices, Inc.
Date: 2018
URL: https://www.analog.com/en/resources/analog-dialogue/articles/jesd204c-primer-part1.html
Abstract. Part 1 of a two-part primer summarising the differences between JESD204B and JESD204C. Introduces the new 64B/66B and 64B/80B link layers, the rationale for mandatory scrambling, the Extended Multiblock structure replacing the LMFC for synchronisation in 64-bit modes, the JESD204 Channel Operating Margin (JCOM) PHY-compliance metric, and the new optional Forward Error Correction.

[14] **D. Jones: JESD204C Primer: What's New and In It for You, Part 2**
Author: Del Jones
Publisher: *Analog Dialogue*, Analog Devices, Inc.
Date: 2018
URL: https://www.analog.com/en/resources/analog-dialogue/articles/jesd204c-primer-part2.html
Abstract. Part 2 dives into the 64B/66B block format, scrambler/descrambler ordering, the link-establishment state machine (sync-header alignment → extended-multiblock synchronisation → extended-multiblock alignment), and the FEC encoder. Details the 26-parity-bit Fire code, the SH_lock state machine, the End-of-Extended-Multiblock (EoEMB) sequence detection, and gives application examples in 5G, radar and electronic-warfare systems.

[15] **M. Jones: JESD204B over Optical Fiber Enables New Architecture for Phased-Array Radars**
Author: Michael Jones
Publisher: Texas Instruments White Paper SLYT663 / TechOnline
Date: 2016
URL: https://www.ti.com/lit/pdf/slyt663
Abstract. Explores using JESD204B's CML physical layer over optical transceivers to extend the link reach beyond the typical few-tens-of-centimetres limit to over 100 m. Discusses antenna-element spacing requirements for L-, S- and C-band radars and the implications for SYSREF distribution and timing alignment when the FPGA is no longer co-located with the data converters.

3.2 Texas Instruments

[16] **TI: What to Know About the Differences Between JESD204B and JESD204C**
Publisher: Texas Instruments White Paper SBAA517
Date: 2020
URL: https://www.ti.com/lit/sbaa517
Abstract. Vendor-neutral white paper explaining the move from 8B/10B to 64B/66B and 64B/80B encoding, the resulting reduction in coding overhead from 20% to 3.125%, the replacement of the ILAS/SYNC bring-up sequence with embedded sync headers, and the implications for board layout, channel loss budgeting and protocol implementation. Includes a side-by-side comparison table that has become a de-facto reference in vendor literature.

[17] **TI: Ready to Make the Jump to JESD204B?**
Publisher: Texas Instruments White Paper SLYY057, Rev. B
Date: 2018
URL: https://www.ti.com/lit/pdf/slyy057
Abstract. Introductory white paper aimed at engineers migrating from parallel LVDS or CMOS data-converter interfaces. Quantifies the pin-count and PCB-area savings, surveys TI's then-current portfolio of JESD204B-capable converters, and walks through clocking, SYSREF generation and FPGA IP-core selection.

[18] **TI: JESD204B Overview (High Speed Data Converter Training)**
Publisher: Texas Instruments Training Material SLAP161, Dallas, TX, USA
Date: 2014
URL: https://www.ti.com/lit/pdf/slap161
Abstract. Slide-deck-style training material introducing the JESD204B standard at a glance: lane rates, subclasses, frame and multiframe structure, character-replacement rules and the link-layer state machine. Companion to SLAP159 (Deterministic Latency) and SLAP162 (Physical Layer).

[19] **TI: JESD204B Deterministic Latency**
Publisher: Texas Instruments Training Material SLAP159
Date: 2014
URL: https://www.ti.com/lit/ml/slap159/slap159.pdf
Abstract. Focused training material on the deterministic-latency mechanism. Explains the role of SYSREF in resetting LMFC dividers, the difference between Subclass 1 (SYSREF-aligned, suitable above 500 MSPS) and Subclass 2 (SYNC~-aligned, restricted to below 500 MSPS due to timing margin), and identifies system classes that genuinely require deterministic latency (DPD loops, AGC loops, multi-antenna systems, phased-array radar, MRI).

[20] **TI: JESD204B Physical Layer (PHY)**
Publisher: Texas Instruments Training Material SLAP162
Date: 2014
URL: https://www.ti.com/lit/ml/slap162/slap162.pdf
Abstract. Companion training to SLAP161/SLAP159 covering the physical layer: CML driver characteristics, eye-diagram requirements, transmitter and receiver equalisation, jitter budgeting and channel-loss limits at 12.5 Gbps.

[21] **TI: Implementing JESD204B SYSREF and Achieving Deterministic Latency with the ADC32RF45**
Publisher: Texas Instruments Application Note SBAA221
Date: 2017
URL: https://www.ti.com/lit/an/sbaa221/sbaa221.pdf
Abstract. Application note for the 3-GSPS RF-sampling ADC32RF45. Provides formulae for deriving the SYSREF frequency for an arbitrary device mode, AC characteristics required of the SYSREF driver, recommended SYSREF capture timing, and a worked example for achieving deterministic latency across multiple converters.

[22] **L. Frenzel: JESD204C: A New Fast Interface Standard for Critical Applications**
Author: Lou Frenzel
Publisher: *Electronic Design* (sponsored by Texas Instruments)
Date: August 2020
URL: https://www.electronicdesign.com/technologies/analog/article/21138848/jesd204c-a-new-fast-interface-standard-for-critical-applications
Abstract. Editorial introduction to JESD204C aimed at system architects. Frames the move to 32.45 Gbps lanes and 64B/66B encoding, and the implications for EMI reduction, against the system requirements of 5G base stations, software-defined radios and electronically steered phased arrays. Editorial caution: the article cites the 1+x14+x15 scrambler, which is the legacy 8B/10B-mode polynomial; the JESD204C 64B/66B link layer uses a scrambler based on 1+x39+x58, compatible with IEEE 802.3.

3.3 AMD / Xilinx

[23] **AMD/Xilinx: JESD204 v7.2 LogiCORE IP Product Guide (PG066)**
Publisher: Xilinx, Inc., San Jose, CA, USA
Document ID: PG066
Date: 2020
URL: https://www.amd.com/content/dam/xilinx/support/documents/ip_documentation/jesd204/v7_2/pg066-jesd204.pdf
Abstract. Definitive product guide for the Xilinx LogiCORE JESD204 IP, supporting JESD204B at line rates from 1 Gbps to 12.5 Gbps (non-standard up to 16.375 Gbps). Documents the transmitter and receiver block diagrams, AXI4-Stream and AXI4-Lite interfaces, clocking topology including SYSREF capture, transceiver-sharing strategies between TX and RX, link test modes, and customisation/constraint flow in Vivado. Mandatory reading for any Xilinx-based JESD204B implementation.

[24] **AMD/Xilinx: JESD204C LogiCORE IP Product Guide (PG242)**
Publisher: AMD/Xilinx
Document ID: PG242 (current revision)
Date: 2024–2025
URL: https://www.amd.com/en/products/adaptive-socs-and-fpgas/intellectual-property/ef-di-jesd204.html
Abstract. Successor IP to the JESD204B core, supporting line rates from 1 Gbps to 32.5 Gbps with 8B/10B or 64B/66B link layers. Fully backwards compatible with JESD204B. Targets Artix UltraScale+, Kintex UltraScale/+, Virtex UltraScale/+, Zynq UltraScale+ MPSoC, and Versal AI Core/Prime devices. The IP requires the Versal Transceiver Wizard or the JESD204_PHY core for PHY-layer integration. The JESD204B core itself was last released for Vivado 2024.1; new designs are directed to the JESD204C core.

[25] **Xilinx: JESD204 PHY v1.0 LogiCORE IP Product Guide (PG198)**
Publisher: Xilinx, Inc., San Jose, CA, USA
Document ID: PG198
URL: https://docs.amd.com/api/khub/documents/tFTWDWC1gGRTtU_itrUrHQ/content
Abstract. PHY-only companion IP that simplifies the sharing of a single MGT channel between transmit and receive cores. Covers debug strategies in simulation (Questa SIM) and on hardware (Vivado lab tools), and provides debug-flow checklists for link bring-up.

3.4 Intel / Altera

[26] **Intel: JESD204B Intel FPGA IP User Guide (UG-01142)**
Publisher: Intel Corporation
Document ID: UG-01142, current revision
URL: https://www.intel.com/content/www/us/en/programmable/documentation/bhc1411117158599.html
Abstract. Reference user guide for the Intel/Altera JESD204B IP, supporting line rates up to 17.4 Gbps. Documents the MAC and PHY split, datapath modes, channel-bonding (x6/xN/feedback compensation), parameter editor, the auto-generated `altera_jesd204.sdc` timing constraints file, and the deterministic-latency implementation guidelines for Subclass 1 and Subclass 2. Covers Stratix V, Arria V, Cyclone V, Arria 10, Cyclone 10 GX and Stratix 10 devices.

[27] **Intel/Altera: Altera JESD204B IP Core and TI DAC37J84 Hardware Checkout Report**
Publisher: Intel/Altera
Type: Application Note (interoperability report)
Date: 2014–2018
URL: https://www.intel.com/content/www/us/en/docs/programmable/683421/current/altera-jesd204b-ip-core-and-ti-dac37j84.html
Abstract. Interoperability report demonstrating end-to-end JESD204B link bring-up between the Altera IP core and the Texas Instruments DAC37J84 quad 16-bit DAC. Documents the transmitter data-link and transport layers, scrambling, Subclass 1 deterministic latency configuration, and the practical lessons learned from a heterogeneous-vendor link.

[28] **Altera/Intel: AN 901: Implementing ADC Dual Link Design with Agilex 7 FPGA E-Tile JESD204C RX IP**
Publisher: Altera Corporation / Intel
Document ID: AN-901
URL: https://www.altera.com/products/ip/a1jui0000049uv7mam/jesd204-fpga-ip
Abstract. Application note describing dual-link JESD204C receive design on Agilex 7 FPGAs using E-Tile transceivers, covering link configuration, PHY parameterisation, and bring-up procedures for dual-link converters such as the AD9213.

[29] **Altera/Intel: AN 967: Multiple Device Synchronization in Digital Phased Array System**
Publisher: Altera Corporation / Intel
Document ID: AN-967
URL: https://www.altera.com/products/ip/a1jui0000049uv7mam/jesd204-fpga-ip
Abstract. Application note targeting digital phased-array radar designs that require deterministic synchronisation across many JESD204B/C converters. Details the SYSREF distribution topology, the use of clock-distribution networks (e.g. LMK04828-class jitter cleaners), and the timing analysis required to guarantee LMFC alignment across boards.

3.5 Cross-Vendor Educational Material

[30] **Comcores / Chip Interfaces: JESD204D Controller IP Core**
Publisher: Comcores ApS / Chip Interfaces
Type: Product Brief / Datasheet
Date: 2024–2026
URL: https://chipinterfaces.com/jesd204d/
Abstract. Publicly documented IP core for the JESD204D revision, supporting, per the vendor's product brief, line rates up to 116 Gbps with PAM4 and 58 Gbps with NRZ, with device-level backward compatibility to JESD204C.01 (64B/66B at 32.5 Gbps) and JESD204B (8B/10B at up to 16 Gbps, a vendor extension beyond the 12.5 Gbps limit of the standard). The product brief documents the three channel-reach classes (XSR/MR/LR), the RS-FEC link-layer option, MCDA-ML support, and the encrypted/source delivery options. Useful as a current snapshot of the JESD204D IP landscape, given that AMD/Xilinx and Intel/Altera have not yet released JESD204D LogiCORE / FPGA IP product guides at the time of compilation.

[31] **SiTime: JEDEC JESD204 Standard: An Overview of Subclasses and Benefits**
Publisher: SiTime Technical Blog
Date: July 2024
URL: https://www.sitime.com/company/newsroom/blog/why-jedec-jesd204-standard-gaining-traction-jesd204b-subclasses-and-what-you
Abstract. Vendor-neutral overview of the JESD204 family from a precision-timing perspective, summarising the historical progression JESD204 → A → B → C, the role of subclasses and the timing requirements they place on the system clock and SYSREF distribution.

[32] **All About Circuits: JESD204B vs. JESD204C: What Designers Need to Know**
Publisher: *All About Circuits*, Industry Article
Date: June 2020
URL: https://www.allaboutcircuits.com/industry-articles/jesd204b-vs-jesd204c-what-designers-need-to-know/
Abstract. Side-by-side comparison article covering coding-efficiency, lane-rate and synchronisation differences between the B and C revisions. Notes the bring-up strategy of starting in 8B/10B and switching to 64B/66B once the link is stable.

[33] **Z. Doleżal: What is the JESD204C Standard for ADCs?**
Author: Zachariah Peterson / Doleżal (Altium)
Publisher: *Altium Resources*
Date: November 2022
URL: https://resources.altium.com/p/what-jesd204c-standard-adcs
Abstract. Concise primer summarising the JESD204C physical-layer parameters, subclass topology with reference diagrams, and typical applications in commercial space and 100 MSPS–1 GSPS+ data converters.

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4 Part C: Peer-Reviewed Research and Academic Papers

[34] **Bellato et al.: A JESD204B-Compliant Architecture for Remote and Deterministic-Latency Operation (IEEE TNS, 2017)**
Authors: M. Bellato, D. Bortolato, F. Gonnella, R. Isocrate, F. Montecassiano, A. Triossi
Publisher: *IEEE Transactions on Nuclear Science*, vol. 64, no. 6, pp. 1297–1303
Date: June 2017
DOI: 10.1109/TNS.2017.2655569
URL: https://ieeexplore.ieee.org/document/7828110/
Abstract. Presents a JESD204B-compliant architecture that operates an ADC remotely from the FPGA over a deterministic-latency high-speed serial link, with application to trigger and data-acquisition (TDAQ) systems for nuclear and sub-nuclear physics experiments. The architecture preserves Subclass 1 deterministic timing despite the geographically distributed transmitter/receiver topology, allowing multiple converters that are remote to one another to remain synchronised.

[35] **Bellato et al.: A JESD204B-Compliant Architecture for Remote and Deterministic-Latency Operation (IEEE RT, 2016)**
Authors: M. Bellato et al.
Conference: *20th IEEE Real Time Conference (RT)*, Padova, Italy
Date: June 2016
DOI: 10.1109/RTC.2016.7543080
URL: https://ieeexplore.ieee.org/document/7543080/
Abstract. Conference precursor to the 2017 IEEE TNS journal paper. Introduces the deterministic-latency remote-ADC concept, presents the FPGA implementation and reports preliminary measurement results from the Padova test bench.

[36] **Yan, Hu, Li: Synchronization of JESD204B-Based ADCs**
Authors: T. Yan, S. Hu, X. Li
Conference: *Proc. ICMMBE 2016*, pp. 321–326 (proceedings title per Atlantis Press record)
Publisher: Atlantis Press
Date: 2016
URL: https://www.atlantis-press.com/proceedings/icmmbe-16/25860719
Abstract. Designs a dual-ADC data-acquisition system using two JESD204B-based AD9680 converters and proposes a general FPGA-based synchronisation method that exploits and controls the deterministic latency of the link to maintain a fixed phase difference between the two channels. Validated with practical phase-coherence measurements relevant to radar signal-processing applications.

[37] **Zhang et al.: Application of Synchronous Acquisition Technology Based on JESD204B in Phased Array Radar**
Authors: W. Zhang, J. Liu, Q. Wang
Conference: *IEEE International Conference on Signal Processing, Communications and Computing (ICSPCC)*
Date: 2018
DOI: 10.1109/ICSPCC.2018.8633139
URL: https://ieeexplore.ieee.org/document/8633139
Abstract. Introduces the principles of phased-array radar and JESD204B in tandem, then analyses the key technologies required for synchronous multi-channel acquisition: SYSREF distribution, LMFC alignment and lane-skew compensation. Reports a working FPGA-based prototype.

[38] **Dolores-Curay et al.: Digital Receiver Modernization Using FPGA and JESD204B for SDR Applications**
Authors: A. Dolores-Curay, J. Sarmiento, M. Milla
Publisher: IEEE Conference (Jicamarca Radio Observatory study)
Date: 2022
IEEE Xplore: Document 10043159 (proceedings details per IEEE Xplore record)
URL: https://ieeexplore.ieee.org/document/10043159/
Abstract. Documents the modernisation of the Jicamarca Radio Observatory main-radar digital-receiver chain. Replaces ageing LVDS-based discrete digitisers with a JESD204B ADC + FPGA design that enables wider bandwidth and prepares the platform for future software-defined-radio operation. Presents the new PCB design, the FPGA IP-core implementation and preliminary tests on a development kit.

[39] **Bhattacharjee et al.: ListenToJESD204B: A Lightweight Open-Source JESD204B IP Core (arXiv, 2025)**
Authors: S. Bhattacharjee, A. Cossettini, M. Magno, L. Benini
Publisher: arXiv preprint arXiv:2508.14798
Date: August 2025
URL: https://arxiv.org/abs/2508.14798
Abstract. Presents an open-source JESD204B Subclass 1 receiver IP core in synthesisable SystemVerilog, released under the permissive Solderpad 0.51 licence and targeting the AMD Xilinx Zynq UltraScale+ ZU19EG. Supports four GTH/GTY lanes at 12.8 Gbps and provides cycle-accurate AXI-Stream output with deterministic Subclass 1 latency. Reports a 79% LUT reduction (107 CLBs / ≈437 LUTs) versus the Xilinx LogiCORE JESD204 IP, with a fixed startup latency of 13 clock cycles (40 ns). The first widely-cited fully-open JESD204B core after the Migen-based LiteJESD204B and the Analog Devices HDL framework.

[40] **Balcells-Ventura et al.: Hardware Acceleration of Digital Pulse Shape Analysis Using FPGAs**
Authors: J. Balcells-Ventura, R. Gernhäuser, R. Krücken, et al.
Publisher: *Sensors*, vol. 24, no. 9, art. 2724
Date: April 2024
DOI: 10.3390/s24092724
URL: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC11086082/
Abstract. Implements real-time Digital Pulse Shape Analysis (DPSA) on a MicroTCA platform using a Xilinx Zynq UltraScale+ MPSoC (NAMC-ZYNQ-FMC AMC board). The JESD204B physical and data-link layers are implemented in HDL, while the transport and application layers, including FIR filtering, constant-fraction discrimination, baseline calculation, peak detection and energy calculation for BC501A scintillator detectors, are implemented in HLS. The Analog Devices HDL framework (GPL-2) is used as the JESD204 stack. Demonstrates the practical use of JESD204B in nuclear-physics instrumentation.

[41] **LiteJESD204B: Open-Source IP Core for FPGAs**
Author / Maintainer: F. Kermarrec, EnjoyDigital project
Publisher: GitHub, ongoing
Date: 2018–present
URL: https://github.com/enjoy-digital/litejesd204b
Abstract. Open-source JESD204B core implemented on the Migen/LiteX framework, supporting Xilinx 7-Series, UltraScale and Lattice ECP5. Verified at line rates up to 6.25 Gbps; the unscrambled mode is documented but not formally verified. Frequently cited as a baseline reference in academic JESD204B work.

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5 Comparison Table: JESD204B vs. JESD204C

The following table consolidates the principal technical differences between JESD204B and JESD204C. Sources: JEDEC JESD204B (2011), JEDEC JESD204C (2017) / JESD204C.01 (2021), TI SBAA517, ADI Analog Dialogue (Jones, 2018, parts 1 & 2), AMD/Xilinx PG066/PG242.

Parameter	JESD204B (2011)	JESD204C (2017 / .01: 2021)
First published	July 2011	December 2017 (errata C.01: December 2021)
Maximum line rate per lane	12.5 Gbps	32.45 Gbps
Signalling	NRZ (PAM2)	NRZ (PAM2)
Link-layer encodings	8B/10B	8B/10B (legacy), 64B/66B, 64B/80B
Coding overhead (typ.)	20% (8B/10B)	3.125% (64B/66B); 25% (64B/80B)
Forward Error Correction	Not specified	Optional Fire code (corrects up to 9-bit burst per multiblock)
Scrambling	Optional	Mandatory for 64B/66B and 64B/80B
Synchronisation primitive	ILAS using K-characters; SYNC~ handshake	2-bit sync header per 66-bit block → Extended Multiblock
Time reference	Local Multiframe Clock (LMFC)	Extended Multiblock counter
Subclasses defined	0, 1, 2	0, 1, 2 (with limits on 0 in 64-bit modes)
Deterministic latency	Yes (Subclass 1 & 2)	Yes (Subclass 1 & 2)
Cyclic Redundancy Check	Not specified	CRC-3 / CRC-12 carried in the 64B/66B sync-bit channel
PHY compliance metric	Eye masks (Class B PHY)	Eye masks plus JCOM (Class C PHY)
Physical-layer driver	CML	CML
Backward compatibility	Compatible with JESD204A in Subclass 0	Fully backward compatible with JESD204B
Typical applications	4G LTE, instrumentation, mid-range radar, JESD204B-over-optical (S/C-band)	5G NR fronthaul, AESA radar, electronic warfare, quantum-control DAQ, SDR at GSPS rates

Notes.

- The 64B/66B link layer is the long-term target for new designs; the 8B/10B mode is recommended for initial bring-up because it is unchanged from JESD204B (TI SBAA517).
- JESD204C does not deprecate JESD204B; both link layers are normative within JESD204C, and AMD/Xilinx ships a single LogiCORE JESD204C IP that handles both.
- The 64B/80B link layer was added to allow vendors to retain the same clocking ratios as 8B/10B while gaining FEC and the new sync structure, useful when re-using existing transceiver primitives.

6 Glossary

This glossary is compiled primarily from the two parallel Analog Devices JESD204 glossaries (cited as the final two entries of this section), expanded with terms used elsewhere in this bibliography. Abbreviations and parameter symbols follow the JEDEC convention.

6.1 Control Characters (8B/10B link layer)

Symbol	Character	Description
/R/	K28.0	Initial Lane Alignment Sequence multiframe start.
/A/	K28.3	Lane alignment.
/Q/	K28.4	Initial Lane Alignment Sequence configuration marker.
/K/	K28.5	Code Group Synchronisation.
/F/	K28.7	Frame synchronisation.

6.2 Abbreviations

CGS Code Group Synchronisation. The 8B/10B link-layer state in which the receiver locks onto the /K/ K28.5 character stream sent by the transmitter prior to ILAS.

ILAS Initial Lane Alignment Sequence. The four-multiframe training sequence that follows CGS in the 8B/10B bring-up flow; carries the link configuration and aligns lanes across the link.

LMFC Local Multiframe Clock. The per-device divider that defines the multiframe boundary; reset by SYSREF in Subclass 1, by SYNC~ in Subclass 2.

LEMC Local Extended Multiblock Clock. The 64B/66B-mode equivalent of LMFC; defines the boundary of an Extended Multiblock.

MCDA Multiple-Converter Device Alignment. The alignment of converter samples *across* multiple converter devices on the same link.

NMCDA No Multiple-Converter Device Alignment. Mode in which converter alignment is *not* maintained across devices.

RBD RX Buffer Delay. Receiver-side elastic buffer delay, expressed as a number of frame clocks; used to absorb lane-to-lane skew while preserving deterministic latency.

EMB Extended Multiblock. The 64B/66B-mode super-structure of E multiblocks (each 32 blocks, each block 66 bits) that replaces the JESD204B multiframe.

EoMB End-of-Multiblock sequence (binary 00001) carried in the sync-bit channel.

EoEMB End-of-Extended-Multiblock identifier bit; signals the boundary between successive EMBs.

CDR Clock and Data Recovery. Receiver-side circuitry that extracts the bit clock from the serial data stream, relying on transition density guaranteed by 8B/10B encoding or by mandatory scrambling of 64B/66B.

CML Current-Mode Logic. The differential output stage used by all JESD204 PHY drivers; replaces LVDS / CMOS used in earlier converter interfaces.

FEC Forward Error Correction. Optional in JESD204C (Fire code), mandatory in JESD204D for PAM4 (Reed-Solomon).

CRC Cyclic Redundancy Check. CRC-3 / CRC-12 carried in the JESD204C 64B/66B sync-bit channel; replaced by RS-FEC error-detection role in JESD204D.

JCOM JESD204 Channel Operating Margin. The PHY-compliance metric introduced with JESD204C Class C PHY, supplementing the eye-mask compliance of Class B PHY.

MCDA-ML MCDA Multiple-Lane. MCDA across both multiple converters *and* multiple lanes per converter.

FMC FPGA Mezzanine Card (VITA 57.1). A common physical form factor for JESD204B/C ADC and DAC daughter cards.

SerDes Serialiser/Deserialiser. The transceiver hard macro (Xilinx GTX/GTH/GTY, Intel Arria/Stratix transceivers) that implements the JESD204 physical layer.

NRZ / PAM2 Non-Return-to-Zero, two-level Pulse Amplitude Modulation. The signalling used by JESD204B/C and the legacy mode of JESD204D.

PAM4 Four-level Pulse Amplitude Modulation. New in JESD204D, raises per-lane line rate to 116 Gbps but has a higher raw bit-error rate that mandates RS-FEC.

XSR / MR / LR Extra-Short-Reach / Medium-Reach / Long-Reach. The three channel-reach classes defined in JESD204D.

MULTIREF The JESD204D Subclass 3 multi-device alignment mechanism that uses a Local Alignment Clock instead of SYSREF; provides alignment but *not* deterministic latency.

6.3 Link Parameters (transport-layer configuration)

L Lane Count. Number of serial lanes on the link.

M Converter Count. Number of converters mapped onto the link.

F Octets per Frame per Lane.

S Samples per Converter per Frame.

NP Total number of bits per sample. The converter resolution N plus optional control and tail bits, recommended to be a whole multiple of 4 bits (padded to the next nibble boundary, so N' = 12 is a valid width for a 12-bit converter). Octet alignment is enforced only at frame level via tail bits.

N Converter Resolution (effective number of bits per sample).

K Frames per Multiframe (8B/10B mode).

HD High-Density User Data Format. Permits a sample to span the boundary between two octets; relaxes alignment but complicates framing. Affects the per-octet substitution rules at the receiver.

E Number of multiblocks in an Extended Multiblock (64B/66B mode).

SCR Scrambling enable flag (0 = disabled, 1 = enabled). Optional in JESD204B; mandatory for JESD204C 64B/66B and 64B/80B.

CF / CS Control Words per Frame Clock cycle / Control bits per sample.

P (JESD204D) Number of payload octets in one FEC code word.

6.4 Clocks

Character clock Clock with which 8B/10B characters and octets are generated.

Conversion clock Clock used by a converter device to perform the A/D or D/A conversion. Equals the converter's sample rate.

Link clock Link parallel clock feeding the link layer. For JESD204B: lane rate divided by 40 or 80. For JESD204C 64B/66B: lane rate divided by 66.

Device clock Master clock supplied to the JESD204 device, from which all other clocks must be derived. In an FPGA context, typically an integer multiple of the frame clock and used directly in link, transport and application layers.

Frame clock Clock rate at which samples are generated or processed. Equal to the conversion clock except for interpolating/decimating DACs and ADCs, where it is slower by the interpolation/decimation factor.

Line clock Clock for the high-speed serial interface (i.e. the serial bit rate / 1).

Local clock A clock generated inside a JESD204 device.

SYSREF Slow source-synchronous clock used to reset device-clock dividers (including LMFC) and thereby achieve deterministic latency in Subclass 1. May be one-shot, gapped-periodic, or periodic. When present, SYSREF is the master timing reference of a JESD204B/C system.

SYNC~ System-synchronous, active-low signal from the receiver to the transmitter used in Subclass 2 for deterministic latency below 500 MSPS, and in 8B/10B mode for synchronisation handshakes generally. Synchronous to the LMFC. > *All clocks inside a JESD204 system must have an integer relationship to one another.*

Physical layer (PHY)
The high-speed transceiver (CML driver, equalisation, CDR). Implemented in the FPGA SerDes hard macro (Xilinx GTX/GTH/GTY, Intel Arria/Stratix transceivers, Versal GTY/GTYP).

Data-link layer Handles 8B/10B (or 64B/66B / 64B/80B) coding, scrambling, character replacement, lane alignment, ILAS or sync-header alignment, and CGS.

Transport layer Handles the mapping between converter samples and framed octets according to the link parameters *L*, *M*, *F*, *S*, *N*, *NP*, *HD*.

Application layer User-defined; implements application-specific signal processing (FIR filters, DDC/DUC, peak detection, trigger logic, etc.). The control-character, abbreviation, link-parameter and clock entries above follow the canonical definitions from Analog Devices' two parallel glossaries:

All clocks inside a JESD204 system must have an integer relationship to one another.

6.5 Source Citations for the Glossary

[42] **ADI: JESD204B Glossary (Wiki)**
Publisher: Analog Devices, Inc., Analog Devices Wiki
Date: Page version approved 13 June 2025
URL: https://wiki.analog.com/resources/fpga/peripherals/jesd204/jesd204_glossary
Abstract. The original ADI Wiki glossary, organised into Control Characters, Abbreviations, Link Parameters and Clocks. The page is being migrated to GitHub-IO and now points readers to the new location below. The 13 June 2025 revision is the latest approved version at the time of compilation.

[43] **ADI: JESD204 Interface Framework Glossary (HDL Documentation)**
Publisher: Analog Devices, Inc., GitHub-IO
Date: 2023–2025
URL: https://analogdevicesinc.github.io/hdl/library/jesd204/index.html
Abstract. The current canonical location of the ADI JESD204 documentation, including the glossary, the 4-layer architectural overview (Physical/Link/Transport/Application), the deterministic-latency discussion for Subclasses 0/1/2, the FPGA HDL support matrix (GTXE2/GTHE3/GTHE4/GTYE4 for AMD Xilinx; GTY/GTYP for Versal; Arria 10, Stratix 10 H-Tile, Agilex 7 F-Tile for Intel), and the licensing terms for the open-source HDL framework (commercial via IP-JESD204 / GPL 2 dual licence). The glossary content is identical to the Wiki source above; this page is the authoritative reference going forward. —

7 Notes on Sources, Access and Coverage

JEDEC standards. The full text of JESD204A, JESD204B, JESD204C, JESD204C.01 and JESD204D is licensed material distributed by JEDEC at https://www.jedec.org after free registration. The specifications are revised periodically and dot-revisions (e.g. JESD204B.01, JESD204C.01) carry editorial corrections. As of December 2023, JESD204D is the current revision; JESD204C.01 (December 2021) remains the relevant errata revision for the C generation and the backward-compatibility target for JESD204D's 64B/66B link layer.

Vendor literature. All Analog Devices, Texas Instruments, AMD/Xilinx and Intel/Altera documents listed above are available without registration from the URLs given. Document numbers (PG066, SBAA517, SLAP161 etc.) remain stable across revisions; check the version date on download. JESD204D-specific FPGA-vendor IP product guides are not yet publicly available at the time of compilation; the Comcores JESD204D Controller IP entry in Part B is the current substitute.

Academic literature. IEEE Xplore papers require institutional access for full text. arXiv preprints and MDPI Open Access papers are freely downloadable. The peer-reviewed body of work on JESD204 is modest, the standard is principally covered by industry literature, but the papers listed in Part C are representative of the FPGA-implementation, deterministic-latency and remote-operation research strands. Peer-reviewed work specifically targeting JESD204D had not appeared by the time of compilation.

Coverage horizon. This bibliography is current as of May 2026. Future JESD204D errata (a JESD204D.01 dot-revision is plausible based on the cadence of previous revisions) and any subsequent revision should be checked at https://www.jedec.org/standards-documents before relying on this document for normative use.

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8 Imprint / Impressum

This bibliography is published online at www.JESD204B.com and www.JESD204C.com for reference purposes. Consult the original normative JEDEC documents for design-compliance work.

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